(Compulsory Question)

9. Answer the questions given below :

(i) Explain plasma enhnaced CVD (PECVD) with suitable example.

(ii) What are the major distinctions between reactive ion etching and parallel plate etching ?

(iii) Why is masking done in fabrication of CMOS transistor ?

(iv) What is the effect of impurities on the oxidation rate ?

(v) How is Chemical Vapour Deposition done ?

3×5=15

Roll No. .... **Total Pages : 04**

J-21-0108

B. Tech. EXAMINATION, 2021

Semester VI (CBCS)

MICROELECTRONICS TECHNOLOGY

EC-605

Time : 2 Hours *Maximum Marks : 60*

The candidates shall limit their answers precisely within 20 pages only (A4 size sheets/assignment sheets), no extra sheet allowed. The candidates should write only on one side of the page and the back side of the page should remain blank. Only blue ball pen is admissible.

Note : Attempt *Four* questions in all, selecting *one* question from any of the Sections A, B, C and D. Q. No. **9** is compulsory.

Section A

1. (a) Justify the statement that silicon based microelectronics is different than micro-fabrication (MEMS fabrication). **7.5**

(b) State various Chemical Vapor Deposition Techniques. Explain in brief any *one* of the techniques of Chemical Vapor Deposition for MEMS device fabrication. **7.5**

2. Justify the need of vacuum pressure in Physical Vapor Deposition (PVD). Explain in brief any *one* of the techniques of PVD for MEMS device fabrication. Also define the terms step coverage and shadowing. **15**

Section B

3. (a) What do you mean by zone refining and how we are able to produce a pure structure of an element from an impure element ? **7.5**

(b) Write down the function of Epitaxy in 1C fabrication. How many types of Epitaxy Growth can be done ? Explain. **7.5**

4. Write down in detail all the steps involved in preparation of Si wafer from a Si ingot produced by CZ process. **15**

Section C

5. How is doping done using Ion implantation ? Draw and explain the working of ion implanter. **15**

6. (a) Does the thickness of the epitaxial wafer pose a problem in epitaxial processing from a stress viewpoint ? Discuss your answers. **7.5**

(b) Describe the principles and uses of rapid thermal, high-pressure and anodic oxidation. **7.5**

Section D

7. (a) What are the differences between CMOS and BiCMOS technologies in fabrication ? **7.5**

(b) Explain the design rules and process parameters of VLSI Technology. **7.5**

8. (a) Explain with suitable diagram fabrication of CMOS. **7.5**

(b) List possible ways of growing on oxide on a substrate without forming oxidation induced stacking faults. **7.5**